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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/998,165	12/03/2001	Tongbi Jiang	M4065.0227/P227-A	7636

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EXAMINER	
PERT, EVAN T	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/998,165	TONGBI JIANG ET AL	
	Examiner	Art Unit	
	Evan Pert	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *31-65* is/are pending in the application.

4a) Of the above claim(s) *33-41 and 49-61* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *31,32,42-47 and 62-65* is/are rejected.

7)☒ Claim(s) *48* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 33-41 and 49-61 are presently withdrawn from consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected species, there being no allowable generic or linking claim. Applicant timely traversed the restriction requirement in the reply entered on January 26, 2005.

2. Applicant's traversal is on the grounds that a serious burden has not been demonstrated to insist on restriction. Yet, applicant makes no admission of a lack of distinctness between the species that have different terms and concepts requiring "different search queries" as stated in MPEP 808.02(c).

3. The restriction to species complies with MPEP 806.04 in that when a generic claim is found allowable, applicant will be entitled to appropriate rejoinder of withdrawn claims drawn to species within the scope of the allowable generic claim.

Claim Objections

4. Claim 31 is objected to under 37 CFR 1.71 because "securing a conductive layer to a backside" is used to mean the more broad term "*forming* a conductive layer on a backside."

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 31-32, 42 and 62-65 are rejected under 35 U.S.C. 103(a) as being unpatentable over any of 1) applicant's admitted prior art, 2) Burr (US 6,218,708), or 3) Wanlass (US 5,422,507), in view of Trueblood (US 4,293,587).

Applicant makes admissions of prior art at pages 1-2 of the specification (i.e. "It is known in the art to maintain...by spacing *the* well plugs..." and "It is common to provide...bias...via well plugs..."). Collectively, the section labeled "Related Art" is reasonably treated as "Applicant's Admitted Prior Art."

Regarding claim 31, applicant's admitted prior art discloses a method of forming a semiconductor device (p. 1, lines 5-6), said method comprising: fabricating at least one electrical element on an upper side of a semiconductor substrate (p. 1, lines 6-7); and fabricating a plurality of bias voltage distribution regions over said upper side of said substrate for receiving a bias voltage and applying said bias voltage to said substrate (p. 1, lines 8-11);

Applicant's admitted prior art and the other two references are generally explicitly silent about "forming a conductive layer on a backside of the substrate," but imply a conductive layer by grounding symbols at the backside of die with bias voltage distribution regions in the transistors at the top.

The Trueblood reference explains "many types of semiconductor chips, particularly memory chips, require for their successful operation an electrically reliable backside contact to the receiving surface to which the chip is attached."

It would have been obvious at the time of applicant's claimed invention to "form a conductive layer on the backside" of applicant's admitted prior art "semiconductor substrate (i.e. die)", or at the substrate backsides of the '708 or '507 references, motivated to form a "vitally important ohmic contact between the backside of the chip and the receiving surface" [col. 1 of the Trueblood reference].

Regarding claim 32, applicant admits well-known transistors as "various transistors" without further written description, which is evidence that the "transistors" are well known. For example, the "memory chips" referred to by the Trueblood reference implicitly have "transistors." The '708 and '507 references show the well-known transistors in their cover figures.

Regarding claim 42, the "providing conductive plugs" limitation is admitted as "common" which is an indication of admitted prior art, can be seen in the cover figure of the '507 reference, and are implied by the figures of the Burr reference [see MPEP 2144].

Regarding claims 62-65, applicant's admitted prior art is silent about "memory device", "DRAM", "logic device" and "processor device", yet indirectly refers to these well known devices as having "various functions" [p. 1, line 1]. The Trueblood reference indicates that "many types of semiconductor integrated circuit chips, particularly memory chips, require an electrically reliable (i.e. conductive layer) for reliable backside contact." [col. 1, lines 6-9].

It would have been obvious to one of ordinary skill in the art to provide a conductive layer on the backside, motivated to achieve "ohmic contact" to the back of the die, "for their successful operation" per the Trueblood reference.

7. Claims 43-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art in view of Hite (US 5,103,283) taken with Davey et al. (US 4,996,171).

The Hite reference shows a method of forming a chip 10 having a plurality of bias distribution regions from Vcc, Vbb, Vss, with a conductive layer on the backside (12) and a "die attach" 8, wherein it would be obvious to distribute Vcc and Vbb as plugs, in view of applicant's admitted prior art that plugs a "known in the art" for distributing bias voltage.

The Hite reference teaches that layer 8 on the backside is a conductive layer as part of a decoupling capacitor, for any type of chip power supply for noise suppression, which is a conductive "die attach" material where the Dave et al. reference discloses a "die attach" that meets the limitations of die attach properties in claims 43-47, with claimed dimensions, thicknesses and resistivity values not presenting patentably significant weight, since there is nothing unexpected disclosed about these design choices of a prior art paste layer used for backside ohmic connection to a die.

Allowable Subject Matter

8. Claim 48 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Evan Pert whose telephone number is 571-272-1969. The examiner can normally be reached on M-F (7:30AM-3:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ETP
October 17, 2005

EVAN PERT
PRIMARY EXAMINER